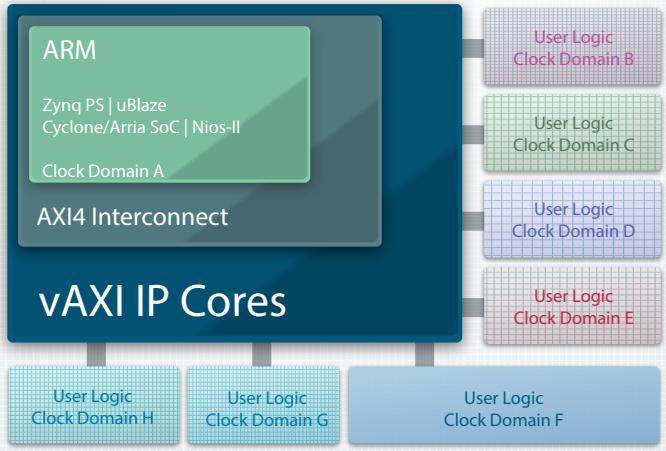
# vAXIom Platform

## Design, Verification and Lab Testing environments for AXI-based designs

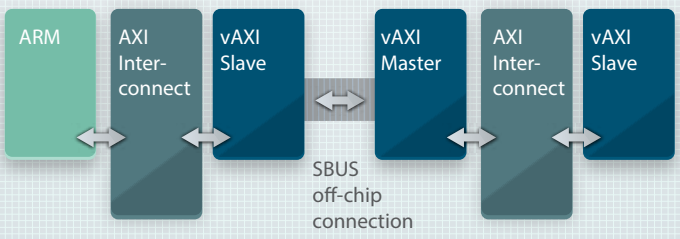
vAXIom platform consists of a portfolio of highly flexible IP cores, enabling fast and easy SoC set up for AXI-based designs. The platform SW automatically generates completely functional RTL verification and synthesis environments, providing an advanced start point for project development. The generated testing environment enables an immediate communication between the on-board design and a computer through JTAG extension. User logic is easily plugged into the environment, using multiple user ports and a variety of available interface protocols. Then, the user logic can easily communicate through vAXI IP Cores and AXI interconnect with other masters and slaves, e.g. Xilinx Zynq PS, uBlaze, Altera SoC HPS, Nios-II, ARM or any custom master or slave. AXI4 memory mapped and AXI-lite protocols are supported. The user ports can be configured to work at different clock domains.




## vAXI-Master/Slave IP Cores and SBUS

vAXI-Slave and vAXI-Master are main building blocks of the environments, acting as bridges between user logic and AXI interconnect. vAXI cores address space and interfaces are highly configurable. A special SBUS interface enables AXI protocol extension to additional FPGAs connected to the primary one, recreating full AXI protocol on the other side. This feature is highly useful for large ASIC SoC prototyping on FPGA.

AXI off-chip extension with SBUS protocol




VSYNC circuits

## Main Features

- >Easy start entry for AXI-based designs
- >Working from day 1 on-board environment
- >Working from day 1 verification environment
- >AXI4 and AXI4-Lite protocols
- >Single and burst accesses over AXI4 interconnect
- >Unlimited user ports with different clocking schemes
- >Different interface types for each user port
  - >Registers (Internal/External)
  - >Memory
  - >Input/output Streaming Buffers
  - >SBUS for off-chip and special protocols
- >Different interface protocols
  - >FIFO (standard/fall-through)
  - >Wishbone
  - >Pulse protocol
- >Separate configuration (data width, buffer depth) of each user port
- >Special interfaces (SBUS) for off-chip communication
- >Low area through internal resource sharing
- >Synthesizable both for FPGA and ASIC
- >Provided with an easy to use user interface facilitating fast configuration and generation
- >Optional double buffer for all types of core interfaces
- >Automatically recognized by leading vendor tools, when connecting to AXI4 interconnect
- >Automatically triggers vendor tools (Vivado, ISE, Quartus) for environments generation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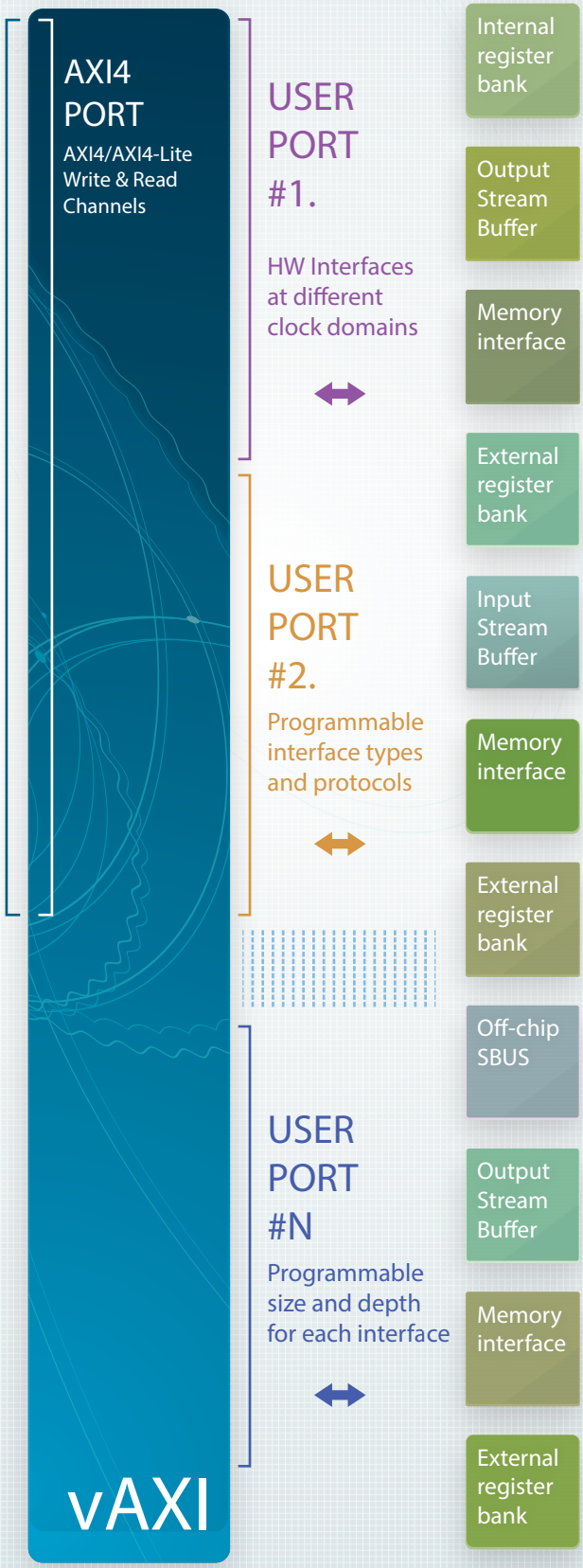
# Top Level Interfaces

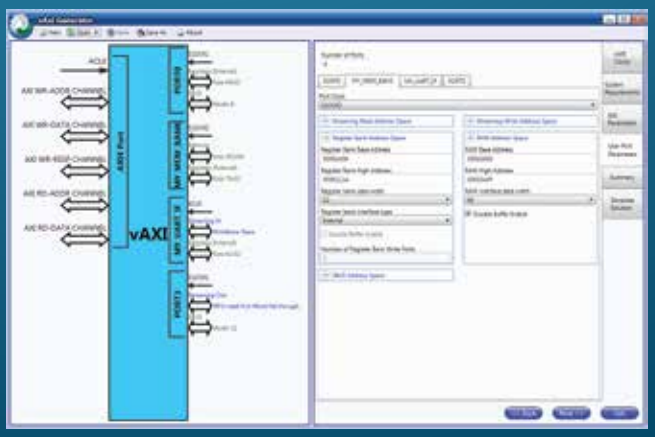
The vAXI IP core top level interfaces consist on one side of AXI4 channels, and on the other side of multiple user ports. Each user port may have multiple different interface types, when each interface type is configured for a required data and buffer sizing, as well as for a required interface access protocol.



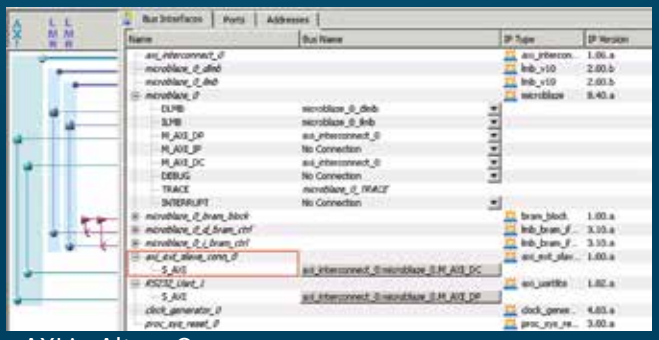

# Integration

vAXIom IP cores are automatically connected to AXI interconnect inside the generated environments, when Xilinx Vivado and Altera QSyS are automatically triggered. The generated Xilinx and Altera environments allow further population by additional vendor and user modules. The auto-generated verification environment provides Bus Functional Model (BFM) fed with a list of user-defined instructions. User Stub modules emulate user logic and respond back to AXI Master Model module for verification. The user replaces the Stubs during user logic integration.

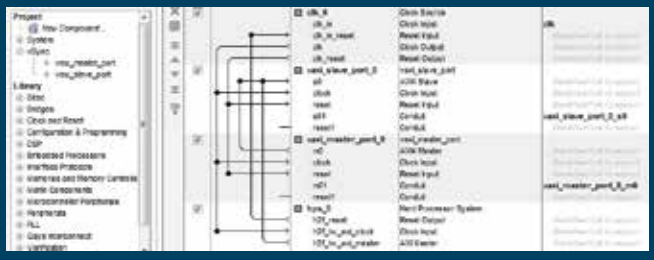
User interface



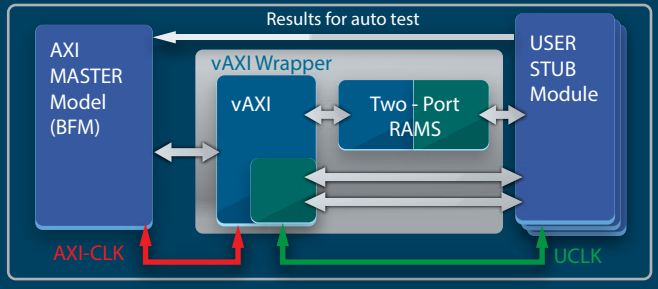

vAXI in Xilinx XPS



vAXI in Altera Qsys



vAXI Verification Environment

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